EXHIBIT 3

Contact

www.linkedin.com/in/krakow (LinkedIn)
www.ti.com/ (Company)

Top Skills

Embedded Systems
Hardware Architecture
Debugging

Ken Krakow

Manager, Hardware Engineering at Roku
Austin, Texas

Summary

• Highly skilled professional with several years of experience in the consumer electronics and semiconductor industry
• Experience in Hardware Systems Architecture and Design
• Familiar with the full chip development cycle
• Broad knowledge and hands-on experience with first silicon bring-up, silicon validation, board bring-up, software development, test, system integration and hardware debug
• Skills as individual contributor, project lead and hands-on manager
• Skills working with and supporting customers
• A valuable combination of knowledge and extensive experience in hardware design, programming, and debugging problems, giving an overall systems view and facilitating systems level solutions

Specialties: Hardware Design, Embedded Systems, Systems Engineering, Validation

Key Skills:
• Detail-oriented system hardware design experience encompassing architecture, high-speed and mixed-signal circuit design, part selection, schematic capture, floor planning, layout, simulation, assembly and test
• Bring-up, debug and validation of new System-on-Chip silicon
• Expert-level assistance on customer designs
• Define and develop firmware for system bring-up, debug and test
• Organize groups and lead teams to achieve important deliverables
• Senior-level design engineer experienced in working across functional teams (marketing, software, applications engineering, IC architecture, IC design, operations) and locations to define and develop products, debug problems, influence design decisions

Experience with:
Hardware Design Tools: Orcad, Pads PowerPCB, Hyperlynx, Viewdraw, Allegro, XTK

Bus Architectures: DDR, USB, ULPI, MII, RMII, PCMCIA, PCI, PCIe, LPC, ISA, 1394, AMBA, AHB/APB, DAP, Trace Bus, EPI, SPI, I2C, I2S, SATA
Processor Architectures: ARM Cortex M3/4, ARM A9, ARM 926, x86, PowerPC
Programming Languages: 'C', x86 & RISC Assembly
JTAG Debuggers Lauterbach, Multi-Ice

Experience

Roku
Manager, Hardware Engineering
April 2014 - Present
Austin, Texas Area

Currently working at Roku managing the Roku TV Hardware team. Working with global partners to ship top quality Roku TV hardware.

Texas Instruments
Senior Systems Designer
May 2010 - March 2014 (3 years 11 months)

• Hardware team lead of five engineers in systems group for ARM Cortex-M MCUs
• Developed board-level systems to support the IC design cycle for 10 silicon revisions and 6 IC package types from emulation through to silicon validation. 32 unique board designs
• Interfaced with architecture and IC design teams to provide system-level context for design decisions, including pin muxing, pad ring, substrate layout, external part requirements
• Worked with marketing, software, operations and applications engineering teams to develop customer-facing reference designs, evaluation boards and documentation
• Schematic and layout reviews for key customers
• On site debug for key customers both in development and production (US-based and overseas)
• Retrofit new silicon into existing customer systems to support software development on new silicon (three unique platforms)
• Worked with IC design, software, and applications engineering to determine root cause for silicon errata and define system level solutions
• System compliance testing of USB 2.0, Ethernet 10/100BT, IEC 61000-4

Trident Microsystems

Systems Design Engineering Manager

February 2008 - May 2010 (2 years 4 months)

Managing Board Design, Validation, Silicon Bring-up, Debug.

Note: Trident Purchased NXP STB

NXP

Systems Engineering Manager

August 2008 - February 2010 (1 year 7 months)

Managing System Integration Validation group responsible for validation of set top box chips.

Conexant BMP group purchased by NXP, August 2008

Conexant

12 years 4 months

Systems Engineering Manager

November 2005 - August 2008 (2 years 10 months)

Managed System Engineering group at Conexant BMP creating set top box designs and validating STB chipsets.

Conexant BMP was then purchased by NXP Semiconductor in August 2008

• Led validation (post silicon) effort for new System-on-Chip MPEG products
• Managed a validation firmware group to develop diagnostics and other software utilities for validating new silicon; managed local engineers as well as directed engineers in Bangalore and Hyderabad, India
• Managed a team of nine engineers and technicians in design, fabrication, assembly, test and shipping satellite set-top box evaluation systems to customers and internal developers
• Helped develop a team of hardware engineers in Bangalore, India, to create and manufacture set-top box evaluation designs
• Defined pad ring order, pad types, and guided BGA substrate design for new chip development

Principle Engineer

May 1996 - November 2005 (9 years 7 months)

• Developed over 15 set-top box evaluation platforms for 6 generations of System-on-Chip designs over the course of 8 years. These set top box designs consisted of a mother board and several daughter boards designed

to support multiple configurations. Boards were 2 to 4 layers, and contained a mixture of analog and digital. Responsibilities included schematic capture, part selection, guiding layout resources, scheduling board assembly, testing and bring-up of systems

• Participated in definition of chip pinout, pin muxing and functional blocks for several chips

• Validation and bring-up of first silicon for numerous MPEG2/MPEG4 decoder chipsets. Used high speed scopes and logic analyzers to validate DDR2, PCI Bus, I/O bus, Audio and Video outputs, high speed data ports, USB (Host/ Device/OTG), Ethernet, UART, SPI, I2C, I2S, PWM and Flash interfaces

• Reviewed customer designs (schematics, layout)

• Led and participated in numerous high profile customer debug efforts

• Designed and implemented an Altera FPGA-based transport stream interface module in Verilog

• Used Hyperlynx and XTK to do signal integrity analysis on various SDRAM and DDR buses

• Defined an emulation strategy. Developed a series of emulation interface boards for use during the decoder chip development. Evaluated, recommended and implemented support hardware for emulation

• Developed reference designs for Brooktree's graphics chips and wrote bring-up and manufacturing diagnostics in 'C'

Advanced Micro Devices

Senior Engineer

April 1995 - May 1996 (1 year 2 months)

System Application and Product Planning for Embeded Processor division. Specifically dealing with the Elan processor family

IBM

Staff Engineer

March 1988 - March 1995 (7 years 1 month)

Poughkeepsie, Boca Raton, Austin

• IBM Power Personal Systems Product Development

• IBM Software Development Solutions

• IBM Main Frame Functional Verification Test

Education

University of Wisconsin-Madison

BSEE,BSCS, Electrical Engineering, Computer Science · (1983 - 1988)